#7/B
Hawkins
9/16/02

Docket No.: LGS/S-0030A

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of		
Joo-Hyong LEE		
Serial No.:	09/955,288	Group Art Unit: 2815
Confirm. No.:	9373	Examiner: Jose R. Diaz
Filed:	September 19, 2001	
For:	LATCH-UP RESISTANT CMOS STRUCTURE	

REPLY AND/OR AMENDMENT
UNDER 37 C.F.R. §§1.111 AND/OR 1.121

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

In reply to the Office Action dated June 19, 2002, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the specification by replacing paragraphs as follows:

A. Specification Paragraphs With Mark-ups to Show Changes Made

The following are mark-ups to show changes made to paragraph(s) starting at page 12, line 9 and ending at page 12, line 16:

As shown in Fig. 2, the CMOS semiconductor device 89 includes two parasitic bipolar transistors 81 and [89] 82. The transistor 81 is an NPN bipolar transistor with source region 71